In the Claims

1. (previously presented) A method for forming shallow trench isolation structures, comprising:

forming a plurality of isolation trenches in a substrate, the isolation trenches separating active areas;

forming an insulation layer outwardly from the substrate, the insulation layer filling the isolation trenches and covering the active areas and substantially conforming to the substrate surface contour;

forming a planarization layer outwardly from the insulation layer, the planarization layer having an outward surface that is substantially flat; and

removing the planarization layer and the insulation layer by a removing process that removes the planarization layer and the insulation layer at substantially the same rate.

2. (currently amended) The method of Claim 1, wherein removing the planarization layer and the insulation layer further comprises:

etching through the planarization layer and the insulation layer together down to a chemical mechanical polishing (CMP) depth outward from the active areas; and

chemically-mechanically polishing from the CMP depth down to [the] a polish stop ~~layer~~ above the active areas.

3. (original) The method of Claim 2, further comprising etching through the planarization layer and the insulation layer at the substantially even rate using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by ten percent or less.

4. (original) The method of Claim 3, wherein the matched etch comprises a resist etch back plasma etch.

5. (original) The method of Claim 2, further comprising etching through the planarization layer and the insulation layer at the substantially even rate using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by five percent or less.

6. (original) The method of Claim 1, wherein the polish stop comprises a polish stop layer disposed outwardly of the active areas and further comprising removing the polish stop layer following the removal of the planarization layer and the insulation layer.

7. (original) The method of Claim 6, further comprising etching a surface of the substrate to selectively remove the polish stop layer thereby forming active areas separated by isolation trench structures formed in the isolation trenches.

8. (original) The method of Claim 6, wherein the polish stop layer comprises silicon nitride.

9. (original) The method of Claim 1, wherein the insulation layer comprises silicon oxide.

10. (original) The method of Claim 1, wherein the planarization layer comprises a resist material.

11. (original) The method of Claim 2, wherein the CMP depth is between 1,000 and 1,500 angstroms above the polish stop.

12. (cancelled)

13. (previously presented) A method for forming an integrated circuit, comprising:

forming a plurality of isolation trenches in a substrate, the isolation trenches separating active areas;

forming an insulation layer outwardly from the substrate, the insulation layer filling the isolation trenches and covering the active areas and substantially conforming to the substrate surface contour;

forming a planarization layer outwardly from the insulation layer, the planarization layer having an outward surface that is substantially flat;

etching through the planarization layer and the insulation layer by an etching process that etches the planarization layer and the insulation layer at substantially the same rate, down to a chemical mechanical polishing (CMP) depth outward from the active areas;

chemically-mechanically polishing from the CMP depth down to a polish stop for the active areas; and

forming integrated circuit devices in the active areas to form an integrated circuit on the substrate.

14. (previously presented) The method of Claim 13, further comprising etching through the planarization layer and the insulation layer using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by ten percent or less.

15. (previously presented) The method of Claim 13, further comprising etching through the planarization layer and the insulation layer using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by five percent or less.

16. (original) The method of Claim 13, wherein the matched etch comprises a resist etch back plasma etch.

17. (original) The method of Claim 13, wherein the polish stop comprises a polish stop layer disposed outwardly of the active areas and further comprising removing the polish stop layer following the chemical-mechanical polishing process.

18. (original) The method of Claim 13, wherein the insulation layer comprises silicon oxide.

19. (original) The method of Claim 13, wherein the planarization layer comprises a resist material.

20. (original) The method of Claim 13, wherein the CMP depth is between 1,000 and 1,500 angstroms above the polish stop.

21. (cancelled)